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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/540,219	01/17/2006	Jean-Bernard Fischer	0579-1097	5286

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EXAMINER	
VAUGHAN, MICHAEL R	

ART UNIT	PAPER NUMBER
2431	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/540,219	FISCHER ET AL.	
	Examiner	Art Unit	
	MICHAEL R. VAUGHAN	2431	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-21,23-30,32,33 and 35-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-21,23-30,32,33 and 35-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/10/09 has been entered.

The instant application having Application No. 10/540,219 is presented for examination by the examiner. Claims 1-9, 11-21, 23-30, 32, 33, and 35-40 have been amended.

Response to Amendment

Claim Rejections - 35 USC § 101

The currently filed amendments overcome the previous *35 USC § 101* rejections.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 17-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 17, it is unclear what is performing the functions of the claim. The amendment has added "said microprocessor executes said computer program comprising". This raises the question as to whether the microprocessor or the computer program comprises a means for calculating and storing. It unclear, as presented, how to determine the scope of the claim. Appropriate correction is required. The dependent claims are likewise rejected for at least the same reasons.

Response to Arguments

Applicant's arguments filed 1/17/06 have been fully considered but they are not persuasive. Examiner respectfully disagrees with Applicant's allegation that the prior art, Naccache fails to the newly amended limitation "inside of said set of instructions". This notion seems to be grounded in a narrow interpretation of the word *set*. In the preamble of the claim, the set of instructions seems to be encompassing all of the instructions of the computer program. That is to say, all instructions belong to the set of

instructions. For the sake of the argument, let us call this set of instructions which encompasses all of the possible instructions of a computer program a **super-set**. This nomenclature is to prevent confusion with the prior art nomenclature. So the claimed invention as broadly interpreted by the Examiner, defines a super-set which is comprises instructions of a computer program. The claimed invention then declares in the last limitation of claim 1 that a jump instruction is one type of the instructions inside the super-set. Therefore the jump instruction is in the super-set of instructions. To reiterate, the word super-set is used to distinguish itself from the word set used by Naccache. Turning to Naccache, the embodiment drawn to in the previous Office Action, is centered on figure 7 and column 13, line 57-column 14, line 60. Starting here from line 57, Naccache's program consists of a first set, second set, and a third set of instructions. Examiner interprets the combination of all three sets of the program to be equivalent to the "super-set" of the claimed invention because it takes all three sets of instructions to present the program. Therefore all of the instructions of El1, El2, and El3, respectfully indicating sets 1-3, are inside of this super-set. Instruction El1-j is defined as a conditional switch which decides the next instruction to execute. Examiner interprets this conditional switch to be equivalent to a jump. Naccache declaring in col. 14, lines 8-13, that no jump exists from the sequence El1-1 through El1-J-1 does not preclude the existence of a jump instruction inside of the super-set. Naccache clearly states that the last instruction El1-j of the set which controls the switching is thus also subjected to hashing (col. 14, lines 32-34). Not only does Naccache teach the jump is "of the set" but so too is the jump inside of the "super-set".

Examiner would also disagree with the assertion that "the amended claim requires the jump to be inside the set of instructions not at the end". In the set of integers {1, 2, 3, 4, 5}, 5 is just as much inside the set as any of the other integers. The word inside does not carry any notion of order within a set.

In conclusion, Examiner still finds Naccache to teach all of the limitations of the claimed invention.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-9, 11-21, 23-30, 32, 33, and 35-40 are rejected under 35 U.S.C. 102(e) as being anticipated by USP 7,168,065 to Naccache et al, hereinafter Naccache.

As per claim 1, Naccache teaches a method of making secure the execution of a computer program (EXE) including a set of at least one instruction, which method is characterized in that it includes:

- a first step (E30), prior to the execution of the computer program, of calculating and storing a first signature (SIG1) representative of the intended execution of the set of instructions (col. 4, lines 25-29),

- a second step (E50), during the execution of the set of instructions, of calculating and storing a second signature (SIG2) representative of the execution of the set of

instructions (col. 4, lines 35-36), and

- a step (E60) of detecting an anomaly in the execution of the set of instructions on the basis of the first signature (SIG1) and the second signature (SIG2) (col. 4, lines 38-39), wherein said set of instructions comprising at least one critical instruction in the form of a jump instruction of any type within the sequence of instructions of said set of instructions (col. 14, lines 33-35).

As per claim 26, Naccache teaches a device for making secure the execution of a computer program including a set of instructions comprising at least one instruction, which device is characterized in that it includes (see abstract):

- a first register (REG1) (col. 4, line 8) for storing a first signature (SIG1) representative of the intended execution of the set of instructions (col. 4, lines 25-29),
- means (22) for calculating and storing in a second storage register (REG2) (col. 6, line 18) during the execution of the set of instructions a second signature (SIG2) representative of the execution of the set of instructions (col. 4, lines 35-36), and
- means (24) for detecting an anomaly in the execution of the set of instructions on the basis of the first signature (SIG1) and the second signature (SIG2) (col. 4, lines 35-36), wherein said set of instructions comprising at least one critical instruction in the form of a jump instruction of any type within the sequence of instructions of said set of instructions (col. 14, lines 33-35).

As per claim 2, Naccache teaches that the first calculation and storage step (E30) is executed during the generation [preparation] of the instructions (AI, AI3) of the computer program (col. 4, line 25).

As per claims 3 and 27, Naccache teaches that the second signature (SIG2) stored during the second calculation and storage step (E50) is retained in memory during the execution of at least one second instruction following the set of instructions (col. 5, lines 4-6 and 64-68). Naccache teaches using one the preceding values in memory to calculate the next value, so therefore it must remain in memory.

As per claims 4 and 28, Naccache teaches the first signature (SIG1) is obtained from the number of instructions in the set of instructions [accounts for each number of the instructions] (col. 9, lines 23-27),

- the second signature (SIG2) is obtained from the number of instructions from the set of instructions that have been executed [numerical value of executed instructions](col. 9, lines 31-35), and in that

the detection step (E60) detects an execution anomaly when the first signature (SIG1) and the second signature (SIG2) are different after the execution of the set of instructions [compare VHn to Vref] (col. 9, lines 60-64).

As per claims 5 and 29, Naccache teaches the first signature (SIG1) is obtained from the number of instructions in the set of instructions [accounts for each number of the instructions] (col. 9, lines 23-27),

- the second signature (SIG2) is obtained from the number [numerical value] of instructions from the set of instructions that have not been executed [next unexecuted

instruction], this second signature (SIG2) being calculated from the first signature (SIG1) [recursive call](col. 9, lines 36-41), and

in that the detection step (E60) detects an execution anomaly when the value of the second signature (SIG2) is not zero after the execution of the set of instructions [compare VHn to Vref] (col. 10, lines 14-19).

As per claims 6 and 30, Naccache teaches that an interrupt of the computer program is triggered when the value of the second signature (SIG2) is below a predetermined threshold (col. 4, lines 40-47).

As per claims 7, Naccache teaches that the first signature (SIG1) and the second signature (SIG2) are retained in memory (col. 1, line 47) during the execution of the program in the same register (REG1) (col. 9, lines 13-17).

As per claims 8 and 32, Naccache teaches the first signature (SIG1) is obtained from the code of a critical instruction of the set of instructions (col. 4, lines 25-29),
- the second signature is obtained from the code of the critical instruction, that code being stored at the same time as or after the execution of the critical instruction [jump] (col. 14, lines 32-35), and in that
- the detection step (E60) detects an execution anomaly when the first signature (SIG1) and the second signature (SIG2) are different after the execution of the set of instructions (col. 10, lines 14-19).

As per claims 9 and 33, Naccache teaches the first signature (SIG1) is obtained from the address of a critical instruction (col. 5, line 51) of the set of instructions, the address being obtained during or after the generation of the executable code of the set

of instructions (col. 4, lines 25-29),

- the second signature (SIG2) is obtained from the address of the critical instruction, that address being stored (E30) at the same time as or after the execution (E30) of the critical instruction (col. 14, lines 32-38), and

- the detection step (E60) detects an execution anomaly when the first signature (SIG1) and the second signature (SIG2) are different after the execution of the set of instructions (col. 10, lines 14-19).

As per claims 11 and 35, Naccache teaches the first signature (SIG1) and the second signature (SIG2) are error detector codes (CRC1, CRC2) calculated from the code or from an address of an instruction of the set of instructions (col. 5, lines 53-58), and in that the detection step (E60) detects an execution anomaly when the first signature (SIG1) and the second signature (SIG2) are different after the execution of the set of instructions (col. 10, lines 14-19).

As per claims 12 and 36, Naccache teaches that the error detector codes are cyclic redundancy check codes (col. 5, lines 53-58).

As per claims 13 and 37, Naccache teaches that the error detector codes are obtained by the logical combination (XOR) of the code or an address of at least one instruction of the set of instructions (col. 5, lines 53-58). Naccache teaches the use of CRC which perform logical combination (XOR included) in order to carry out the operation. Examiner is not giving XOR patentable weight here as the syntax implies XOR as an example of logical combination.

As per claims 14 and 38, Naccache teaches the first signature (SIG1) and the second signature (SIG2) are respectively obtained during the generation and the execution of the instructions from at least two elements chosen from:
the number of instructions in the set of instructions,
the **code** of at least one instruction of the set of instructions (col. 5, lines 45-51),
the **address** of at least one instruction of the set of instructions (col. 5, lines 45-51), and an error detector code calculated from the code or an address of at least one critical instruction of the set of instructions, the address being obtained during or after the generation of the executable code of the set of instructions (col. 5, lines 53-59), and in that the detection step (E60) detects an execution anomaly when the first signature (SIG1) and the second signature (SIG2) are different after the execution of the set of instructions (col. 10, lines 14-19). Naccache teaches using the code and address as hash inputs thus two criteria from the list are chosen.

As per claims 15 and 39, Naccache teaches that it includes a step (E70) of destroying at least a portion of the system on which the computer program is executed, this step of destroying being made when an execution anomaly is detected in the detection step (col. 4, line 45).

As per claim 16, Naccache teaches in that the first signature (SIG1) is generated automatically [already generated before execution of program] (col. 4, line 25-30).
As per **claim 17**, Naccache teaches a device for processing a computer program including a set of at least one instruction, characterized in that it includes means (12) for calculating and storing a first signature (SIG1), the first signature (SIG1) stored in a

memory and the first signature is representative of the intended execution of the set of instructions prior to the execution thereof (col. 4, lines 25-30), said set of instructions comprising at least one critical instruction in the form of a jump instruction of any type within the sequence of instructions of said set of instructions (col. 14, lines 33-35).

As per claim 18, Naccache teaches the first signature (SIG1) [Vref] are adapted to calculate and store information obtained from the number of instructions of the set of instructions (col. 9, line 65 - col. 10, line 5).

As per claim 19, Naccache teaches the means (12) for calculating and storing the first signature (SIG1) are adapted to obtain and store information obtained from the code of a critical instruction [jump] of the set of instructions (col. 14, lines 33-35).

As per claim 20, Naccache teaches means for generating executable code from the computer program (col. 8, lines 35-36).

As per claim 21, Naccache teaches the means for calculating and storing the first signature (SIG1) are adapted to obtain and store information obtained from the address of a critical instruction (col. 5, line 51), the information being obtained of the set of instructions by the means (14) for generating executable code (col. 8, lines 35-40).

As per claim 23, Naccache teaches that the means (12) for calculating and storing the first signature (SIG1) are adapted to calculate and store information obtained from an error detector code (CRC1) calculated from the code or an address of at least one instruction of the set of instructions (col. 5, lines 53-58).

As per claim 24, Naccache teaches that the error detector code (CRCI) is a cyclic redundancy check code (col. 5, line 57).

As per claim 25, Naccache teaches that the error detector code is obtained by a logical combination (XOR) of the code or an address of at least one instruction of the set of instructions (col. 5, lines 53-58). Naccache teaches the use of CRC which perform logical combination (XOR included) in order to carry out the operation. Examiner is not giving XOR patentable weight here as the syntax implies XOR as an example of logical combination.

As per claim 40, Naccache teaches a microcircuit card [smart card] characterized in that it includes a securing device according to claim 26 (col. 6, lines 27-35).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL R. VAUGHAN whose telephone number is (571)270-7316. The examiner can normally be reached on Monday - Thursday, 7:30am - 5:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Vu can be reached on 571-272-3859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. R. V./

Examiner, Art Unit 2431

/Syed Zia/
Primary Examiner, Art Unit 2431